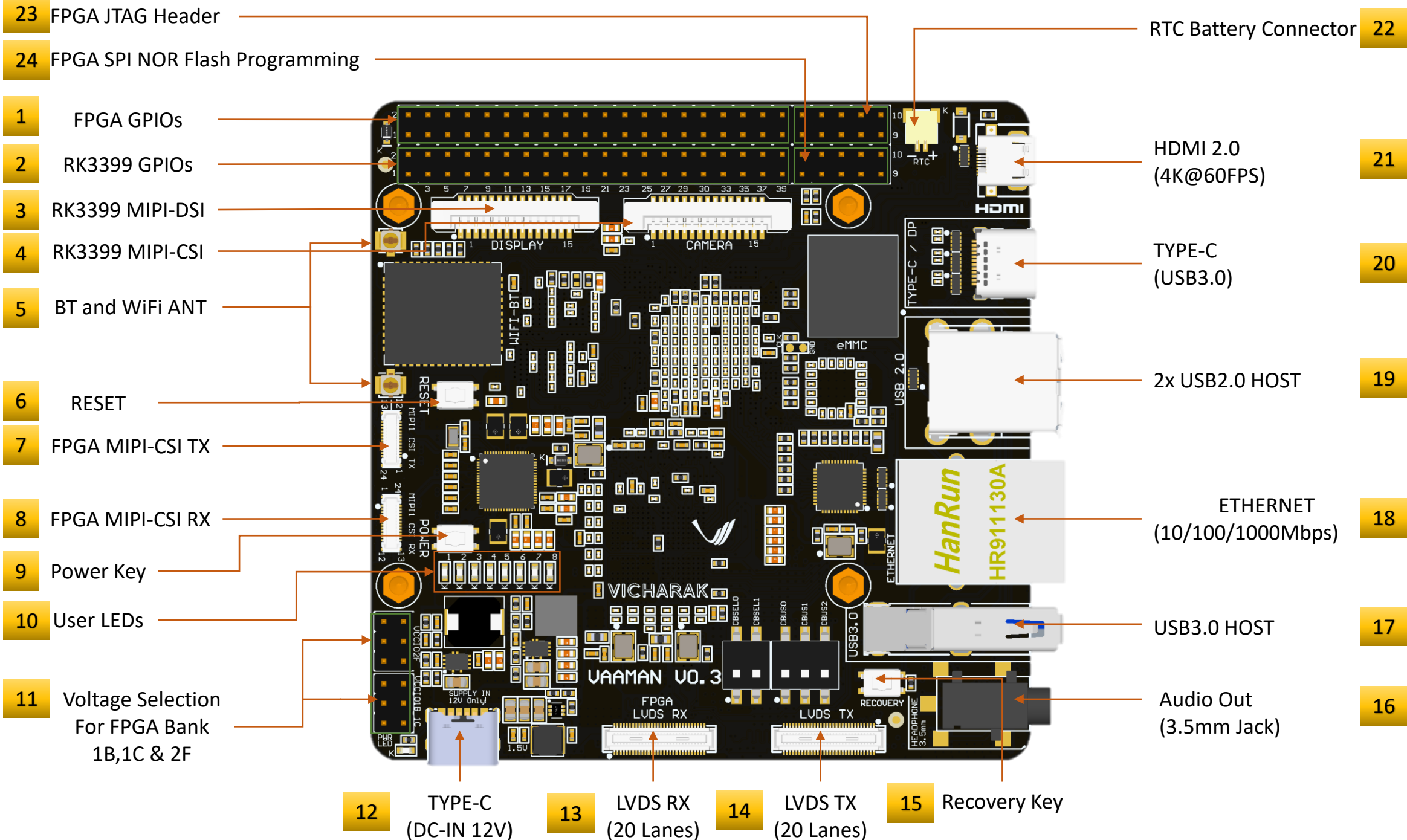
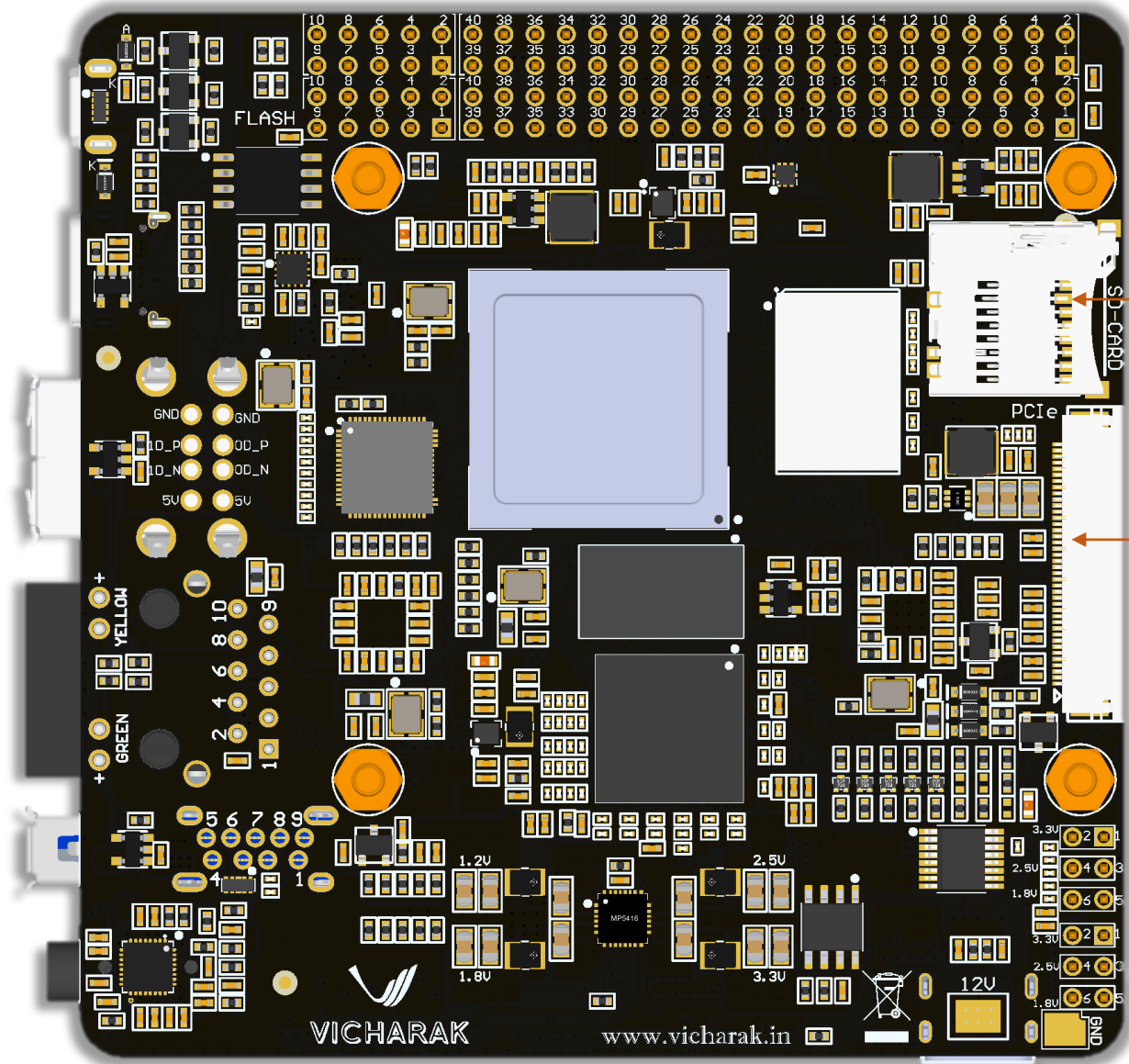


# Revision History

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Document Number	Revision Number	Description	Revision Date
	001	Initial Release	May 2023
	002	Updated RK3399 GPIOs Header pins	July 2023
	003	Page added FPGA Internal Clock Sources	Oct 2023

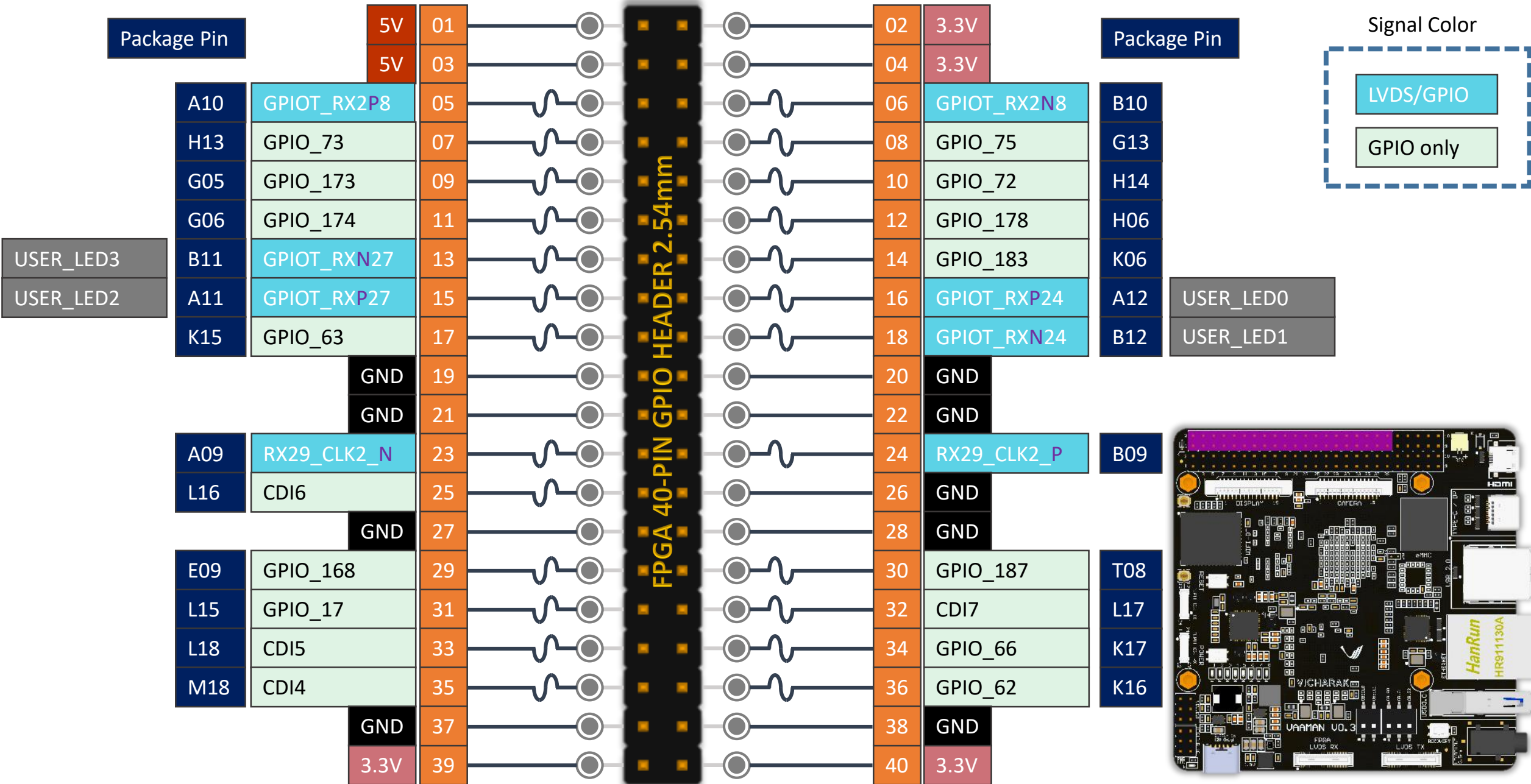




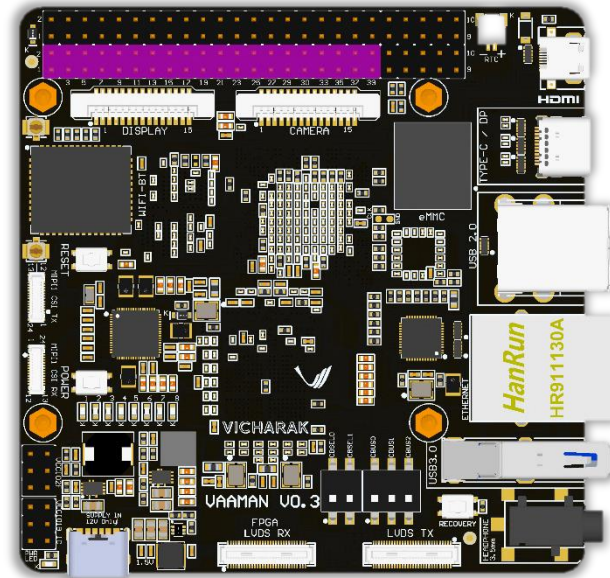
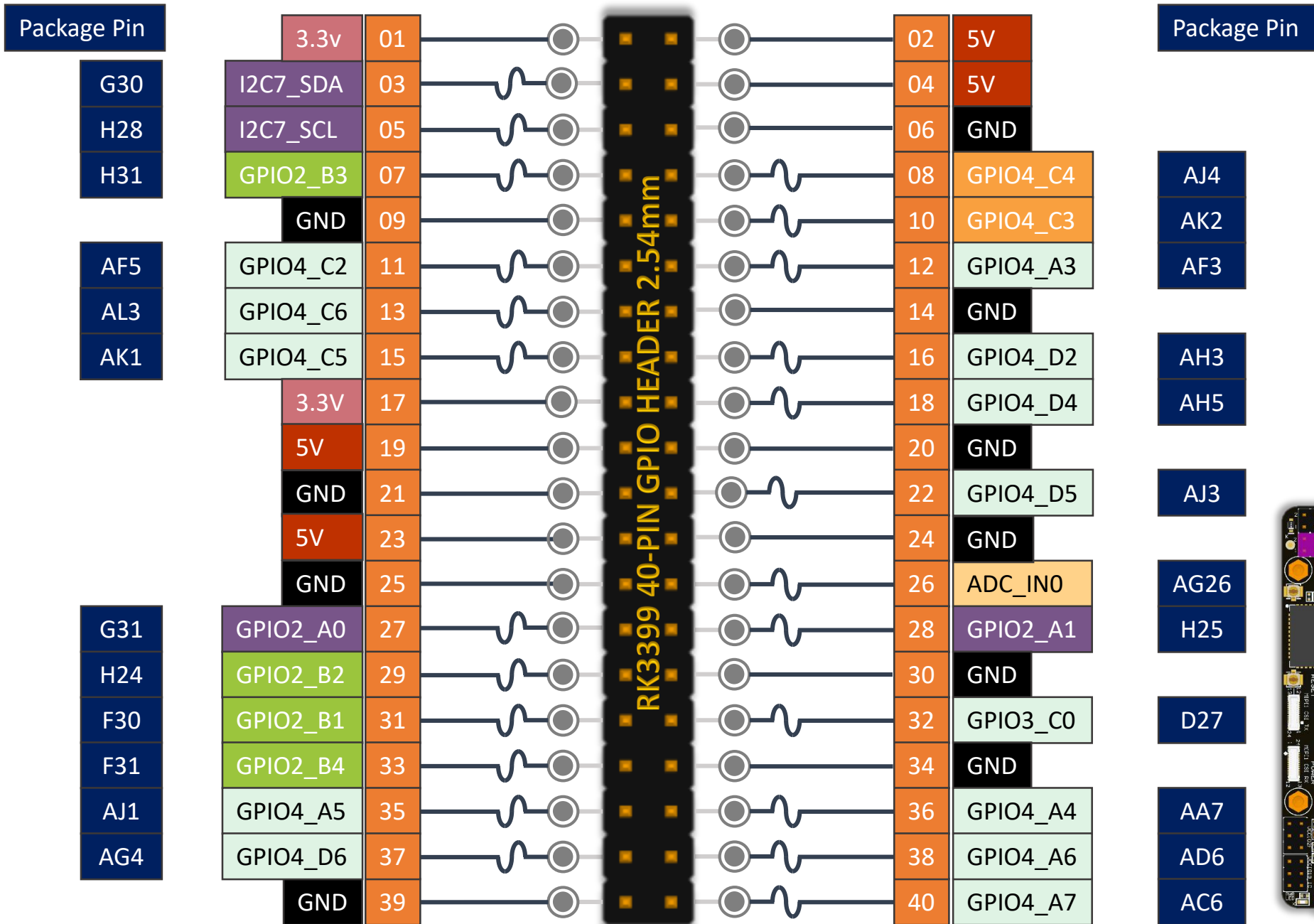
MicroSD Card 25

PCIe (FPC Connector) 26

# 1 FPGA GPIOs

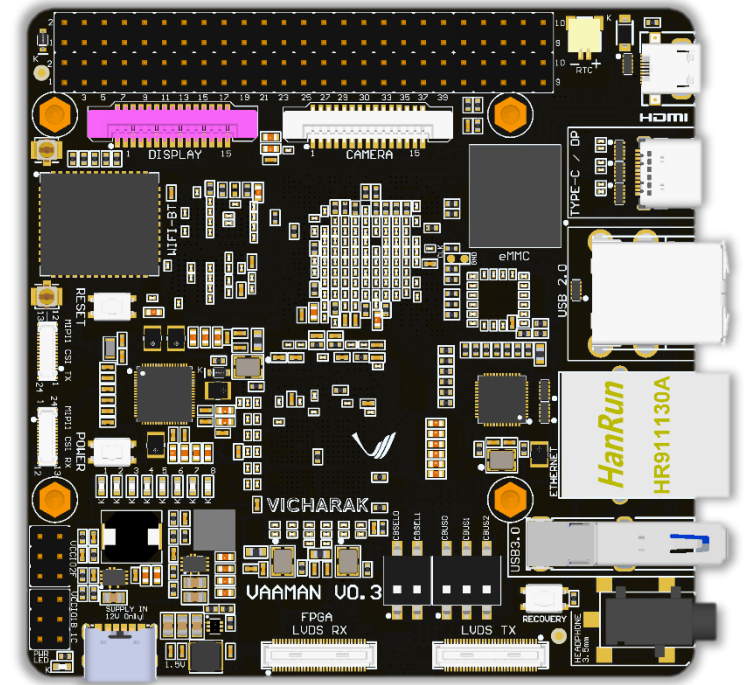
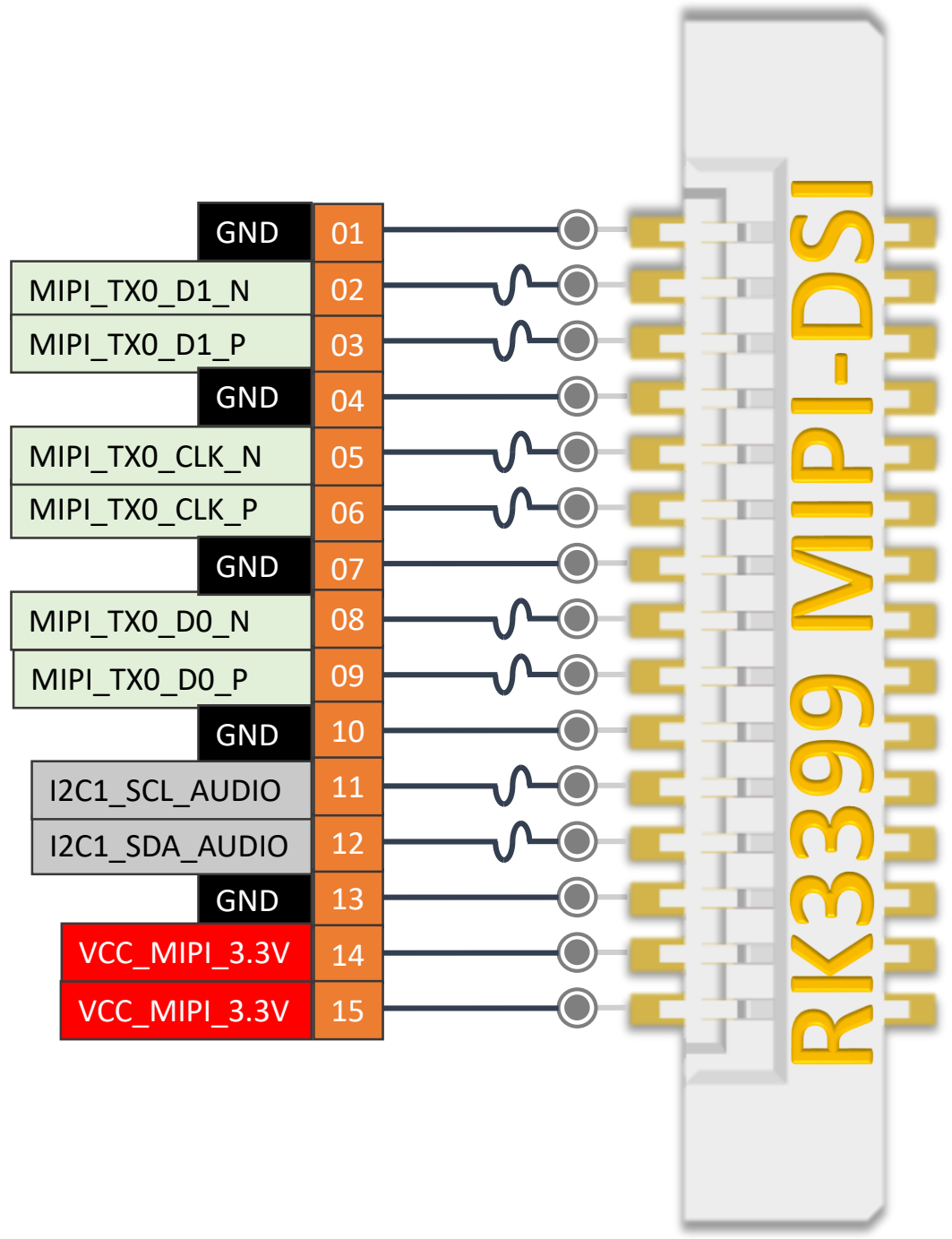


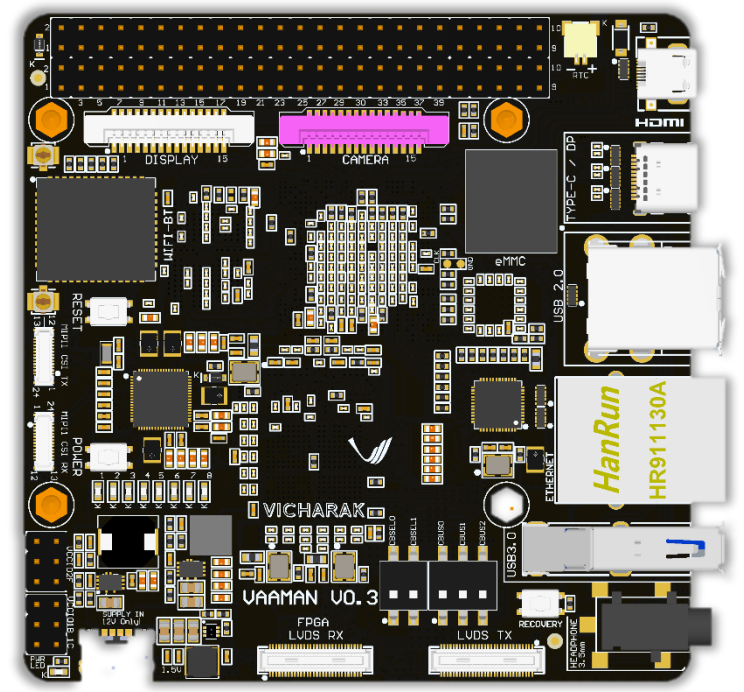
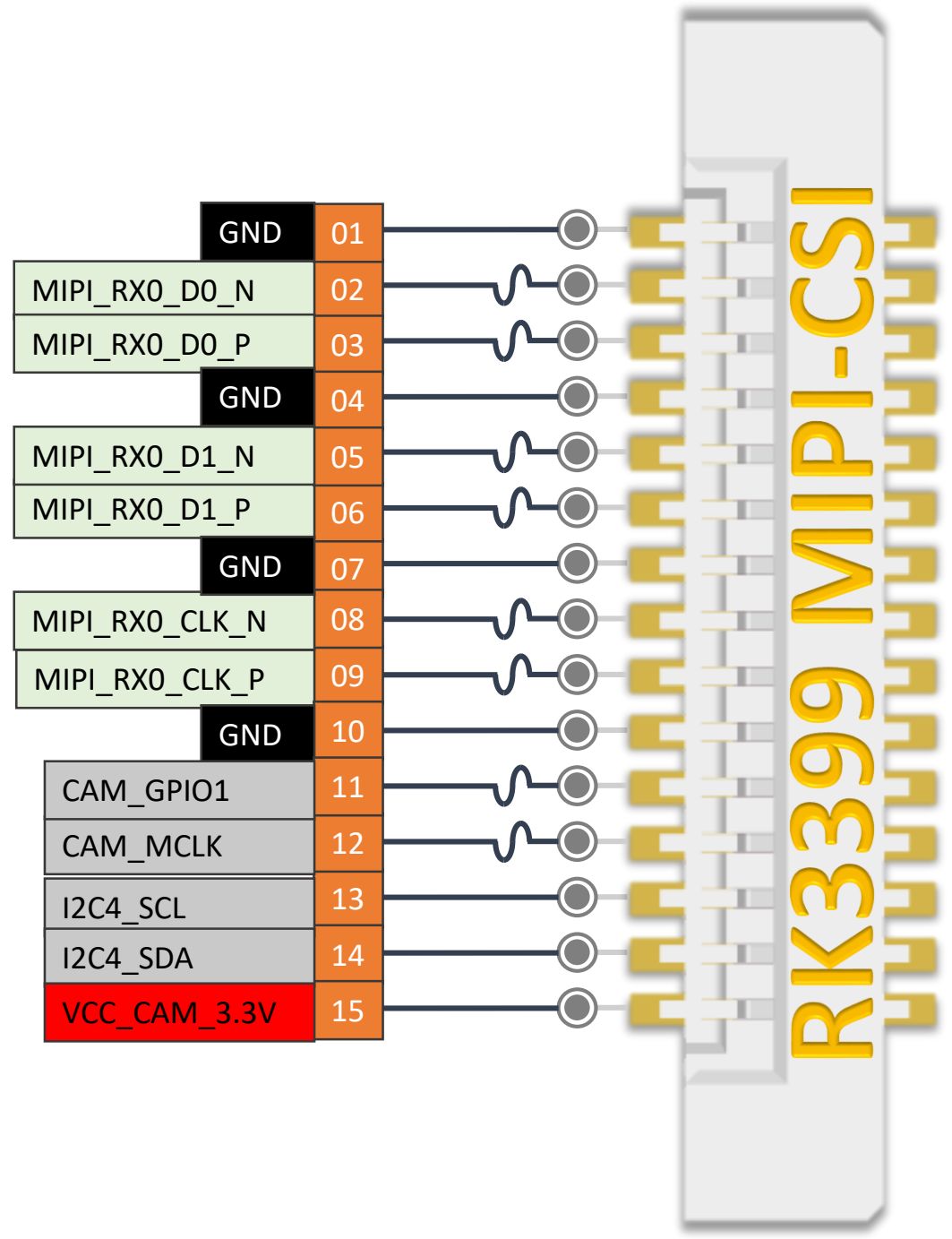
## 2 RK3399 GPIOs



Package Pin
AJ4
AK2
AF3
AH3
AH5
AJ3
AG26
H25
D27
AA7
AD6
AC6

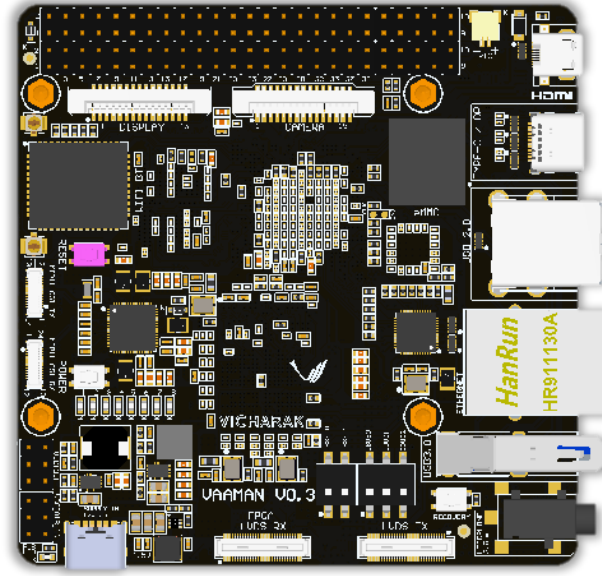




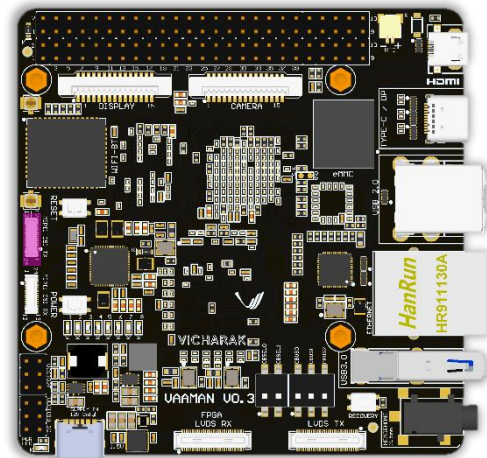
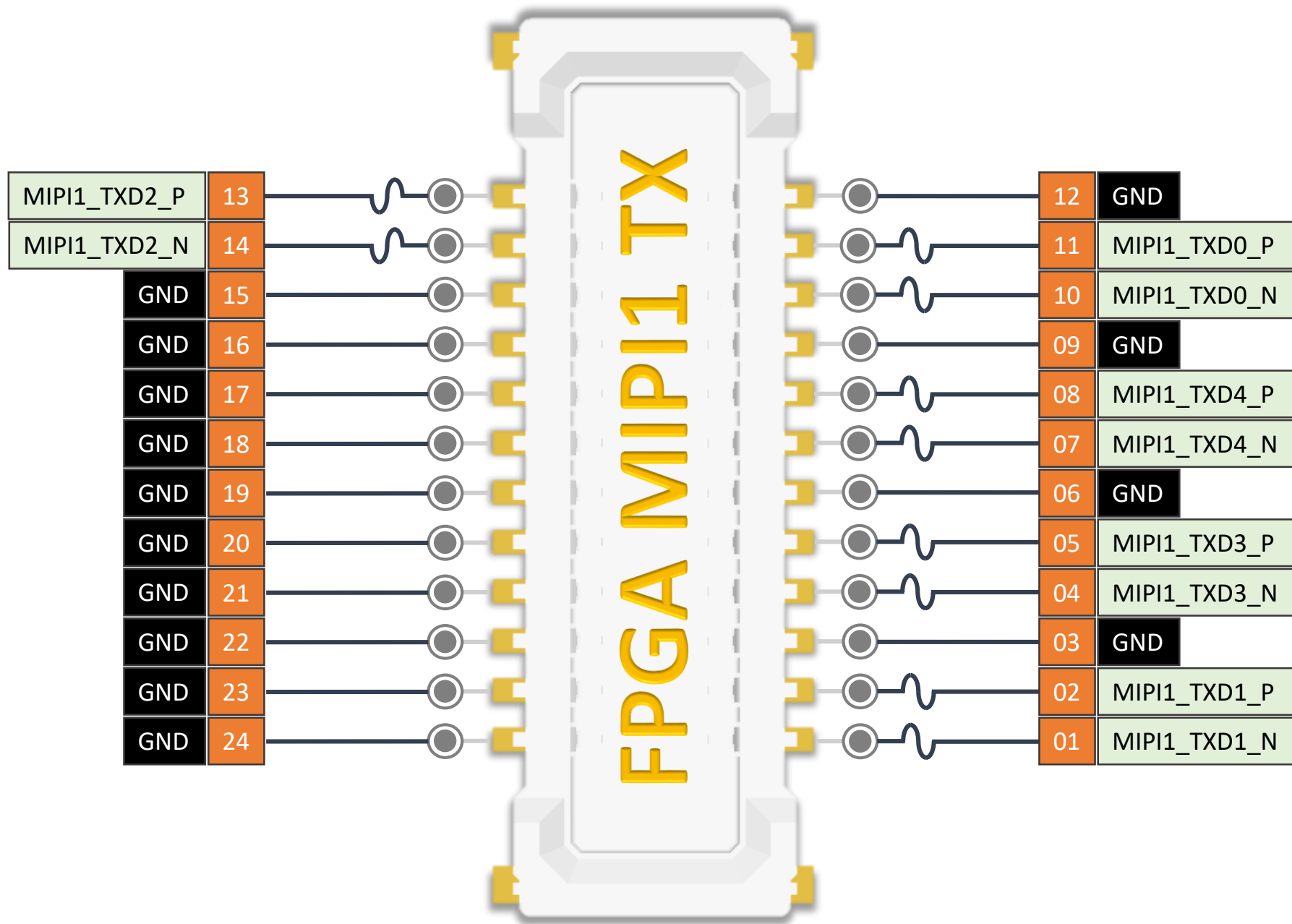


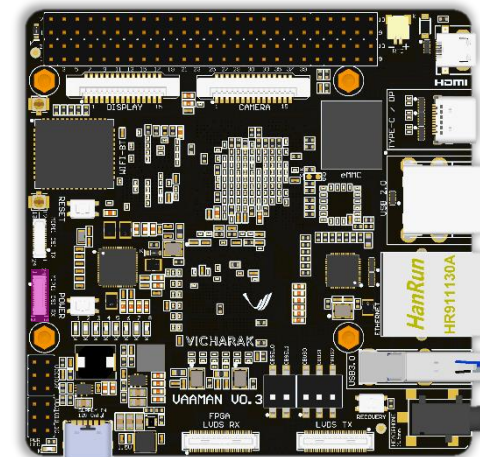
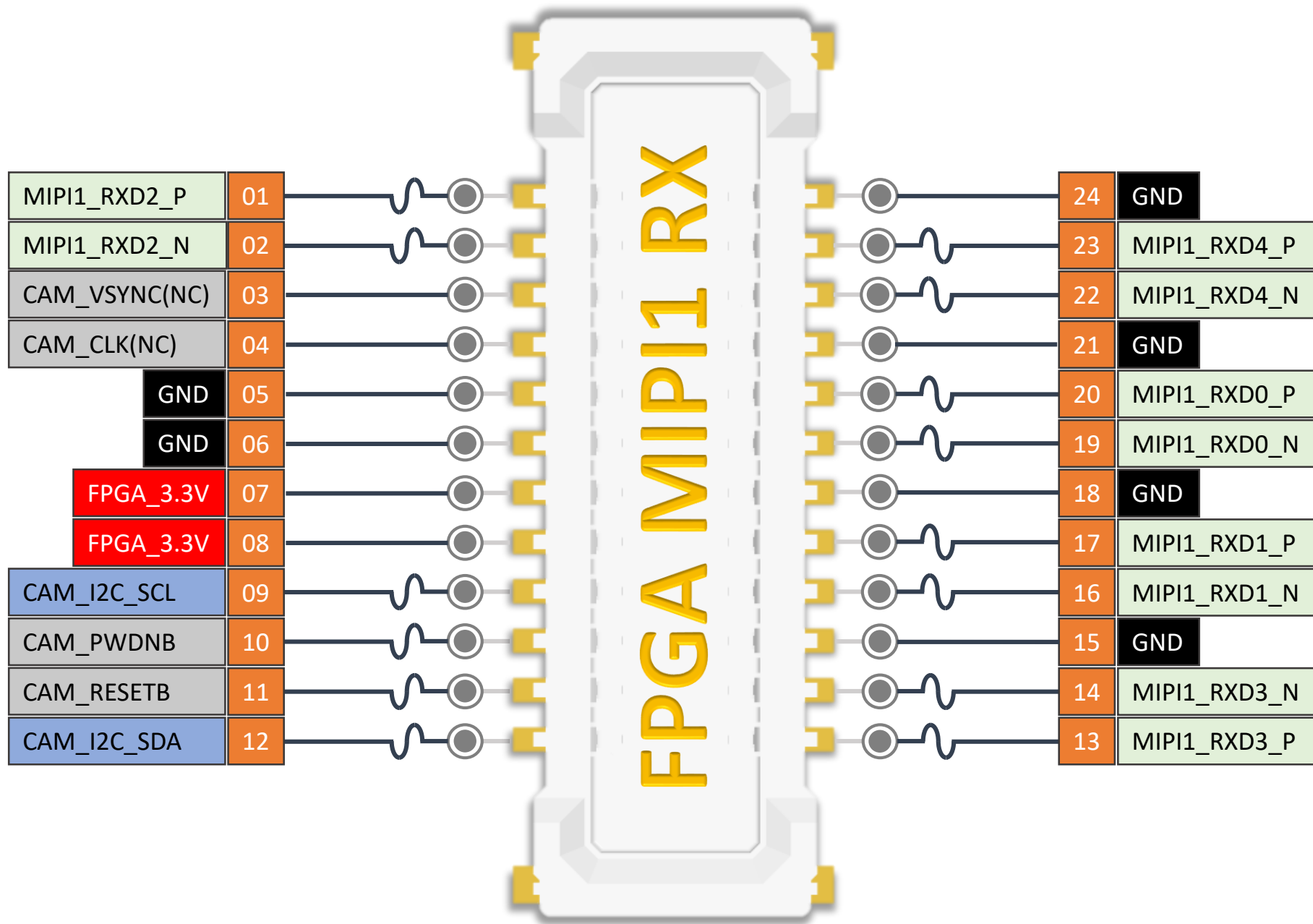


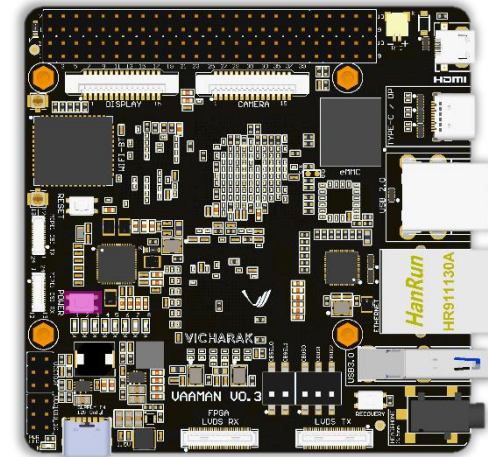
Board **Reset** Push-Button





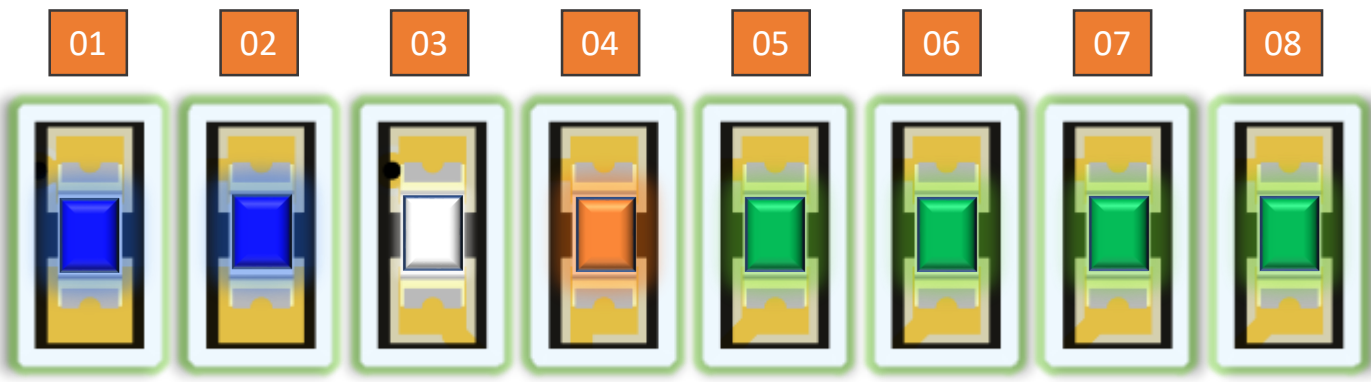
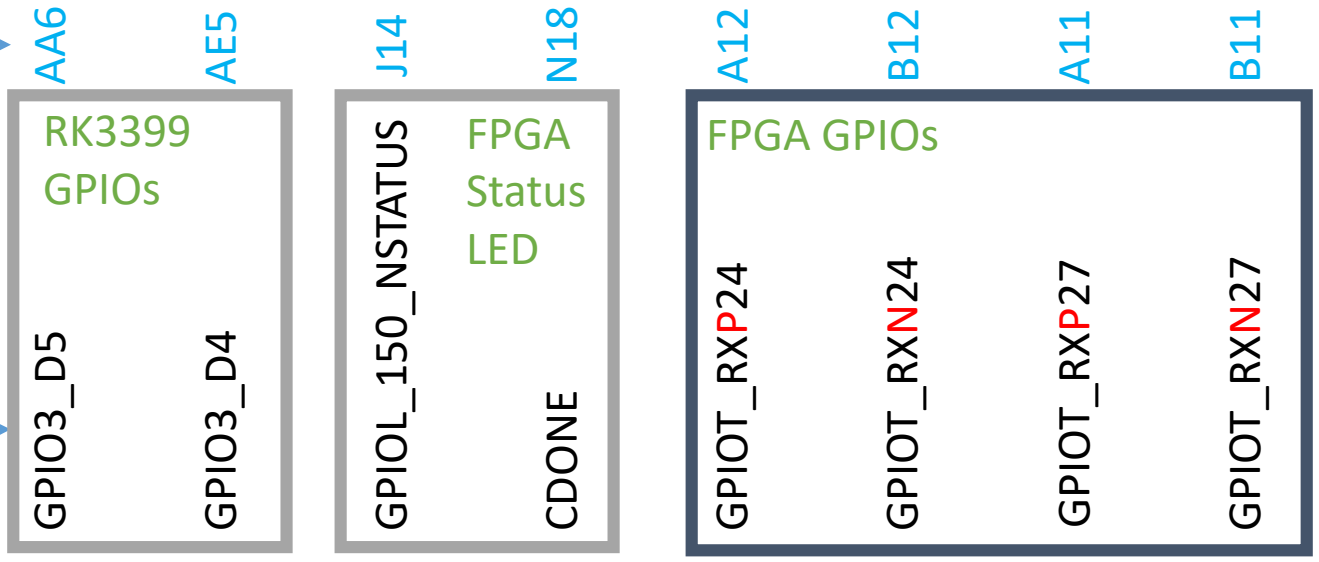






PIN NUMBER

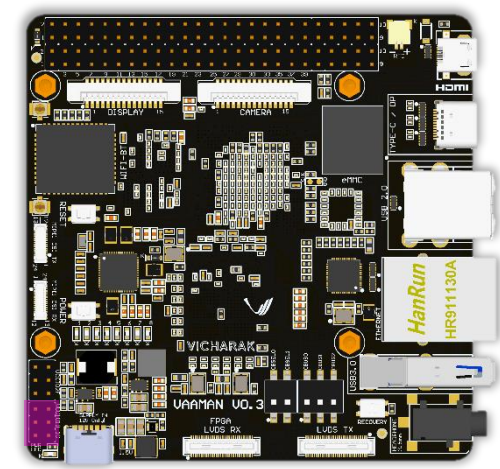
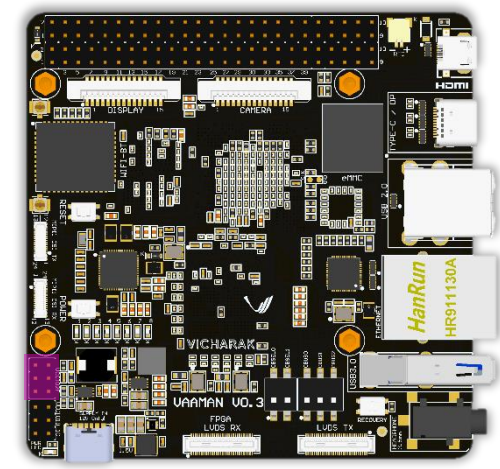
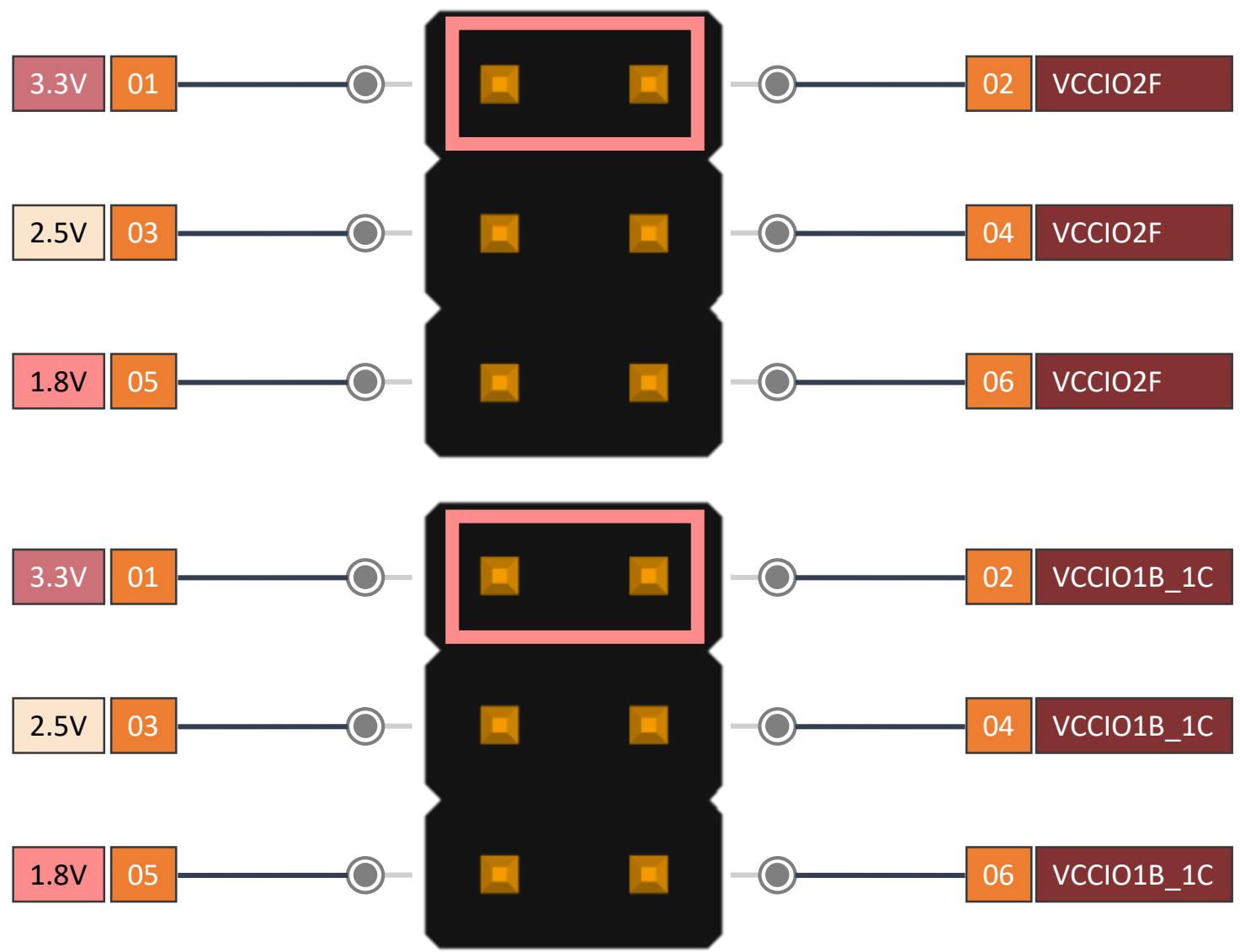
PIN NAME



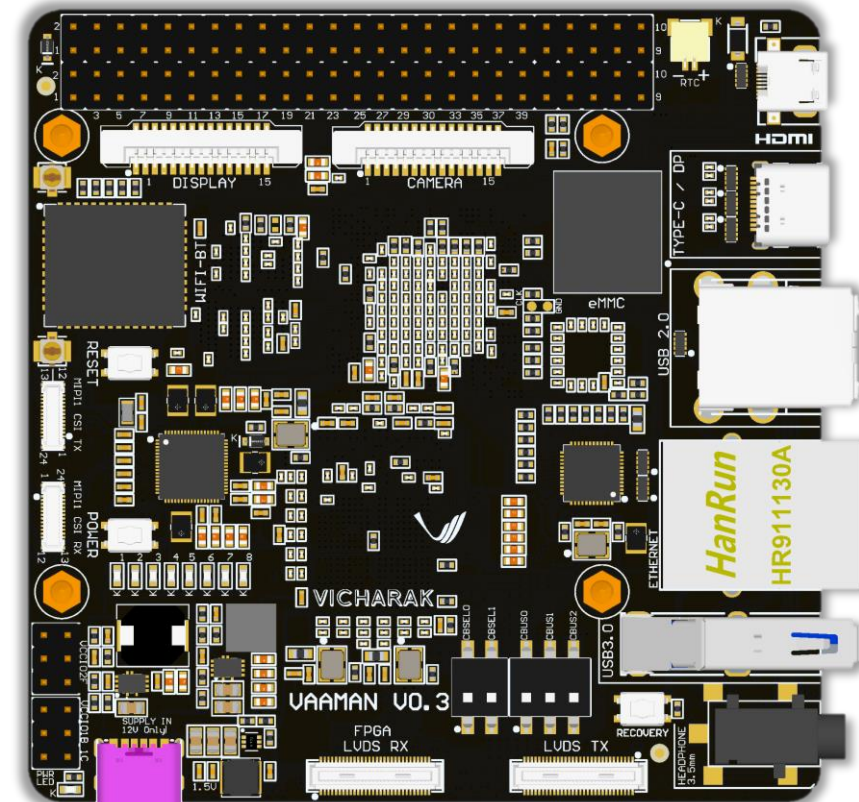
01	Active HIGH	Blue LED
02	Active HIGH	Blue LED
03	Active LOW	White LED
04	Active HIGH	Orange LED
05	Active HIGH	Green LED
06	Active HIGH	Green LED
07	Active HIGH	Green LED
08	Active HIGH	Green LED

RK3399 USER LEDs

FPGA USER LEDs



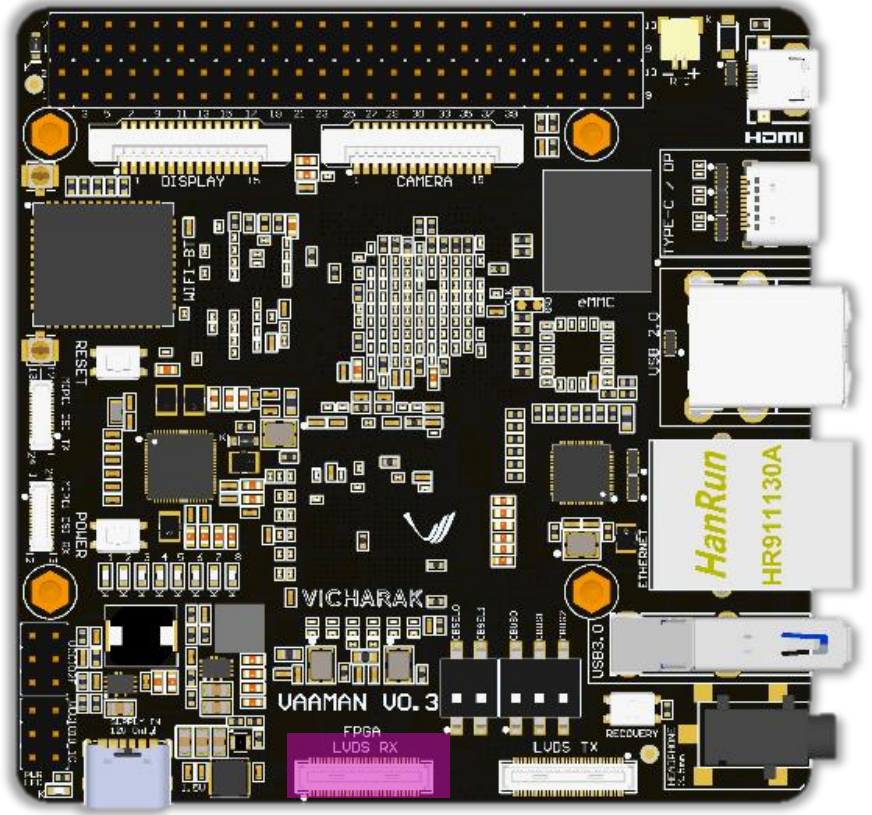
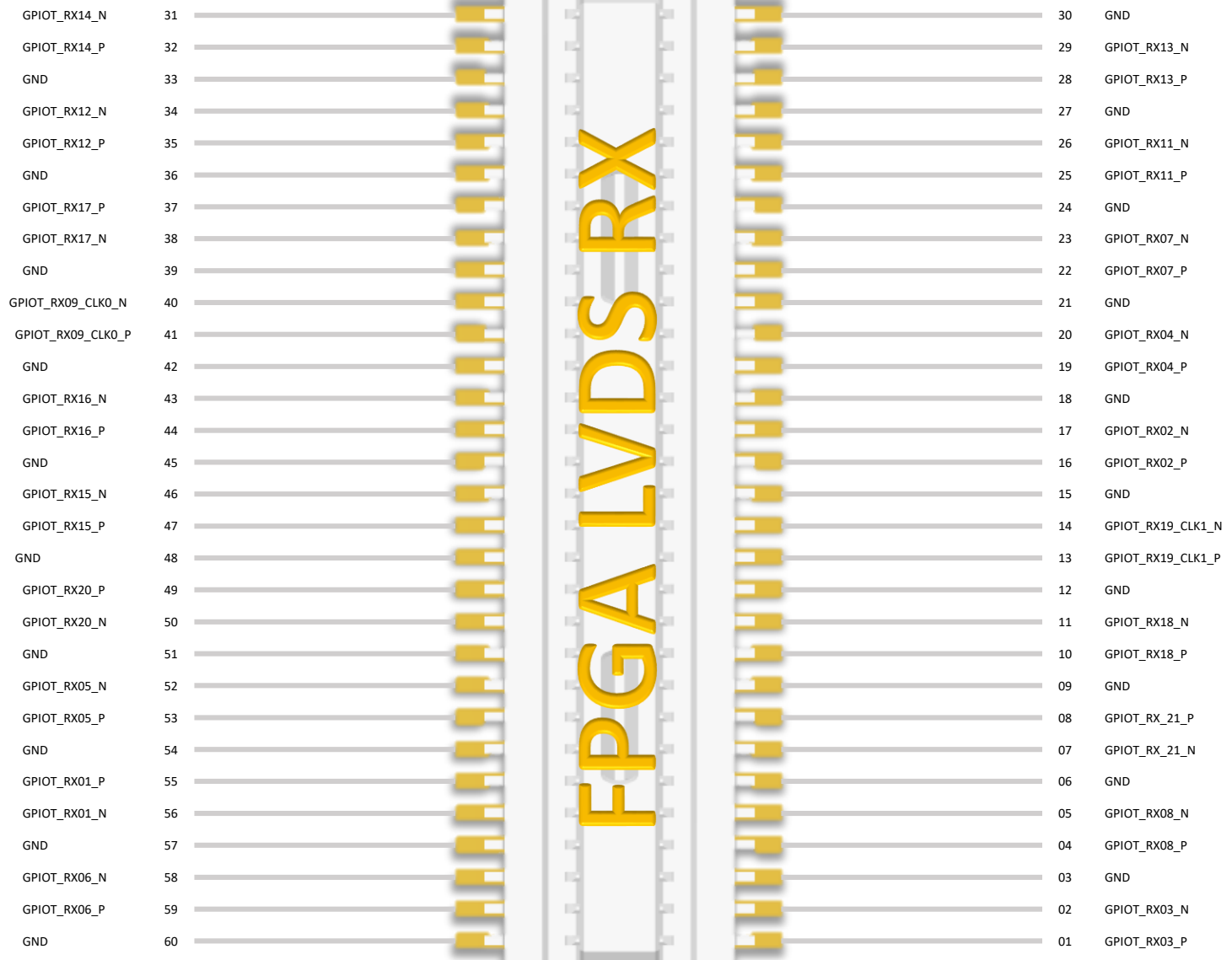
Jumper	VCCIO1B_1C (J2)	VCCIO2F (J3)
Connect pins 1 and 2	3.3 V (default)	3.3 V (default)
Connect pins 3 and 4	2.5 V	2.5 V
Connect pins 5 and 6	1.8 V	1.8 V

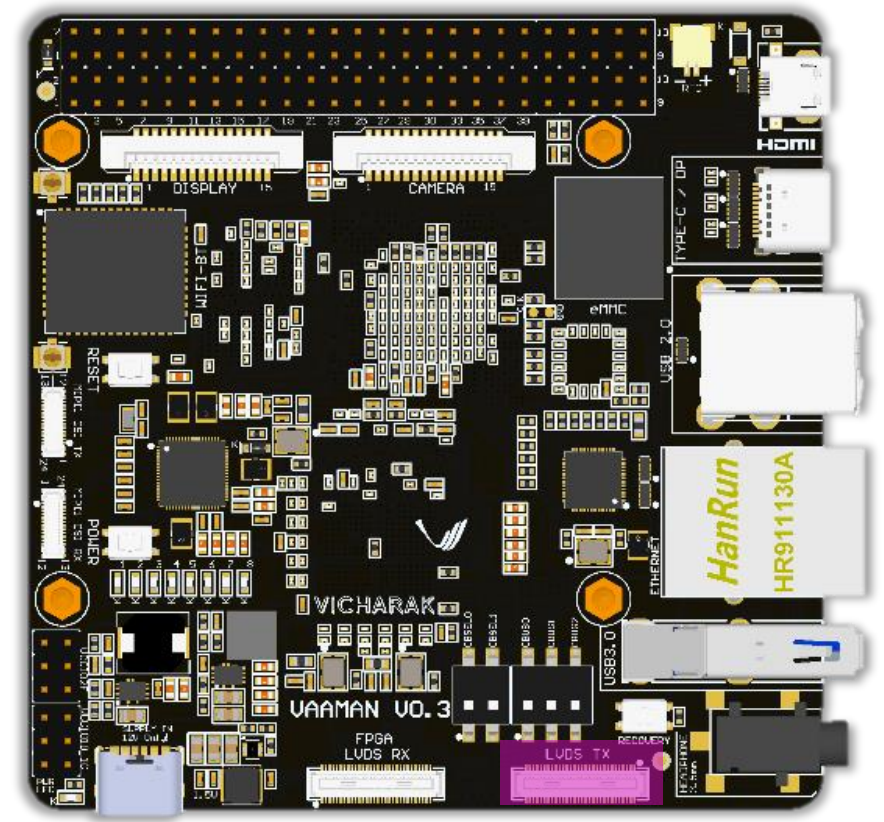
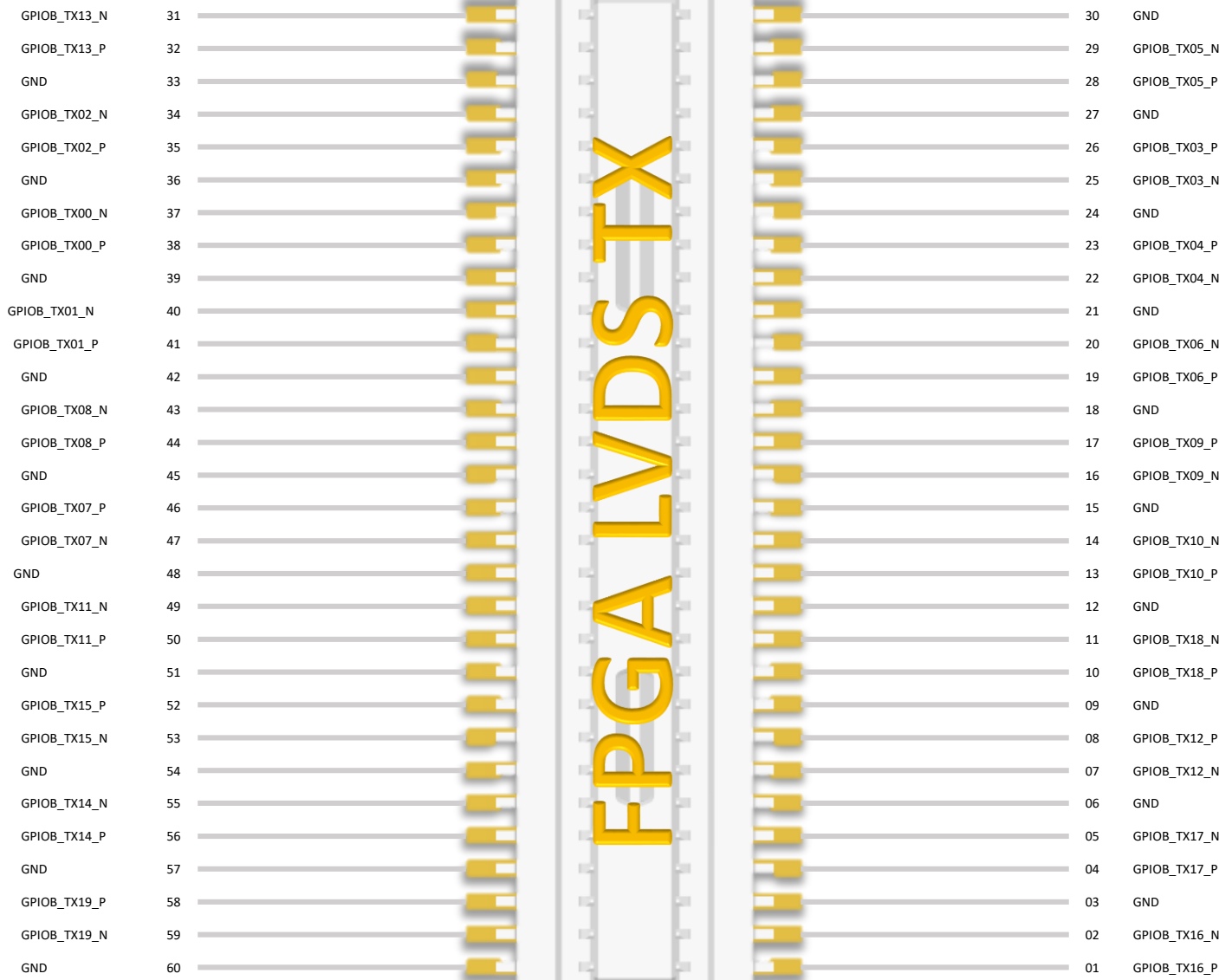


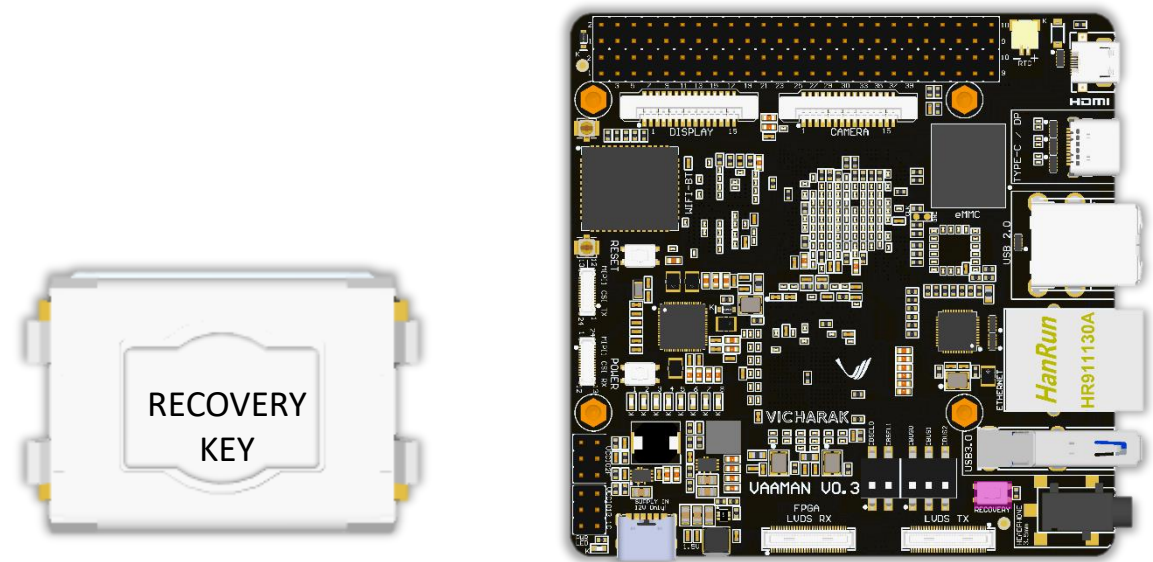
USB PD, support USB Type C PD 2.0, 9V/2A, 12V/2A  
Qualcomm® Quick Charge™: Supports QC 3.0/2.0 adapter, 9V/2A, 12V/1.5A



# LVDS RX (20 Lanes)



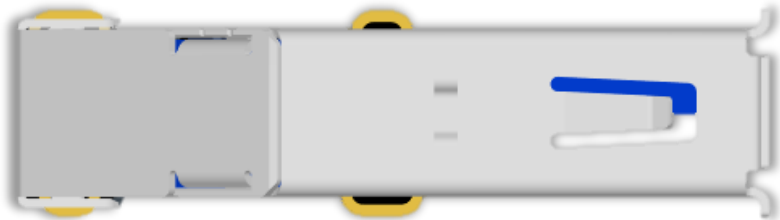




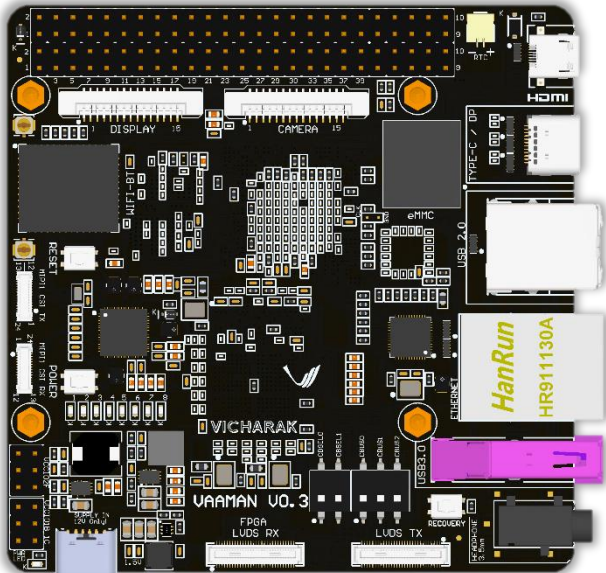
RECOVERY push button to allow user to easily flash over USB the on-board eMMC storage.







USB3.0 HOST

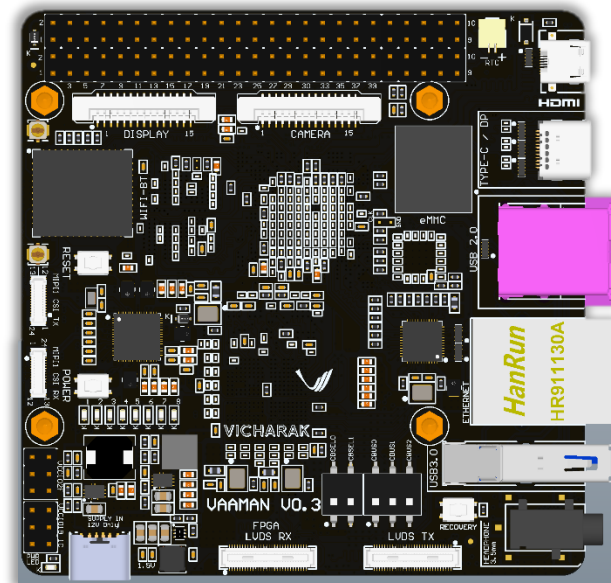


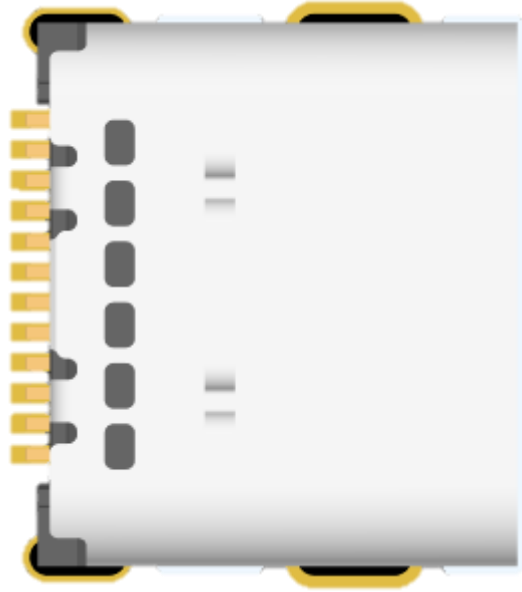




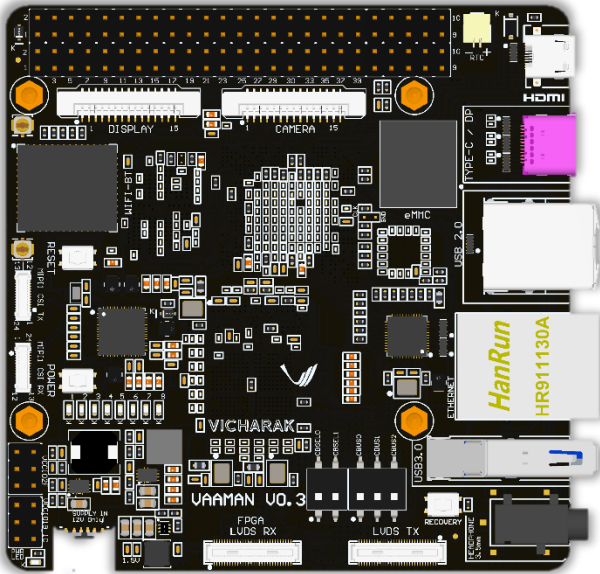


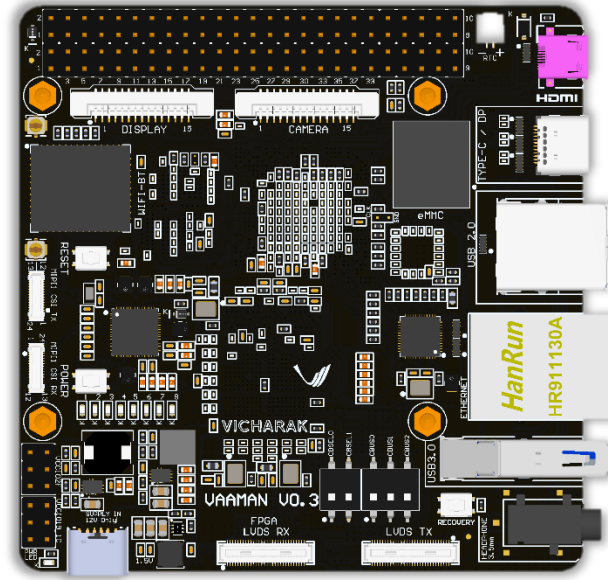
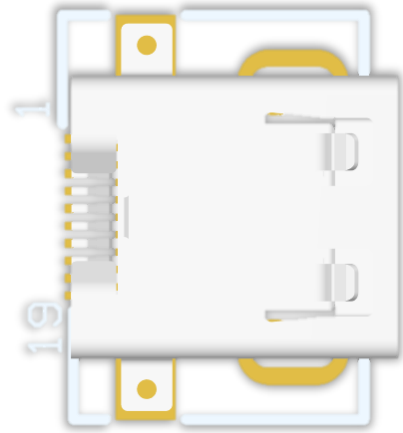
2x USB2.0 HOST

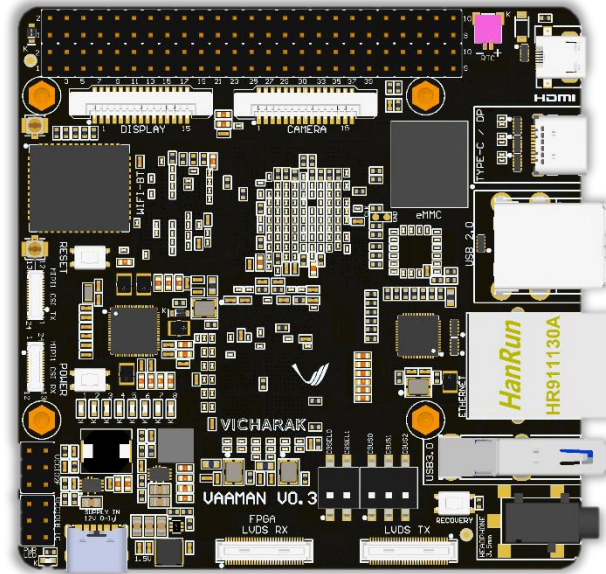
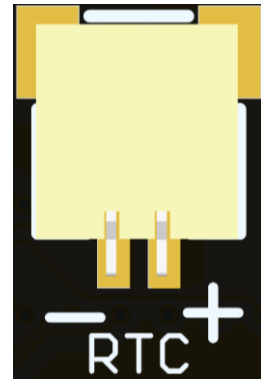


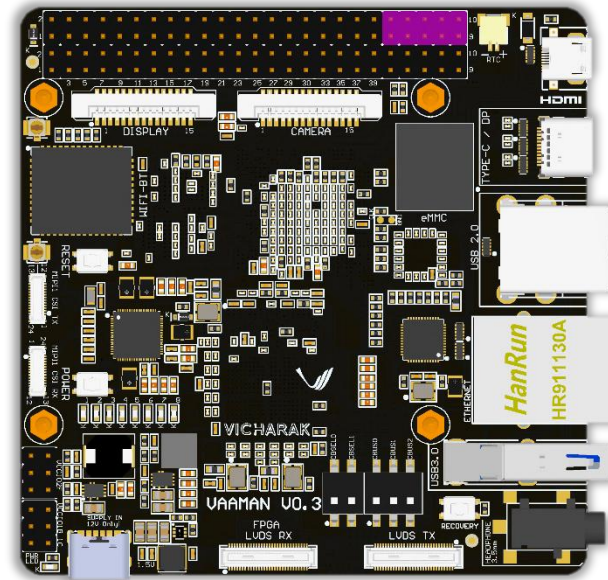
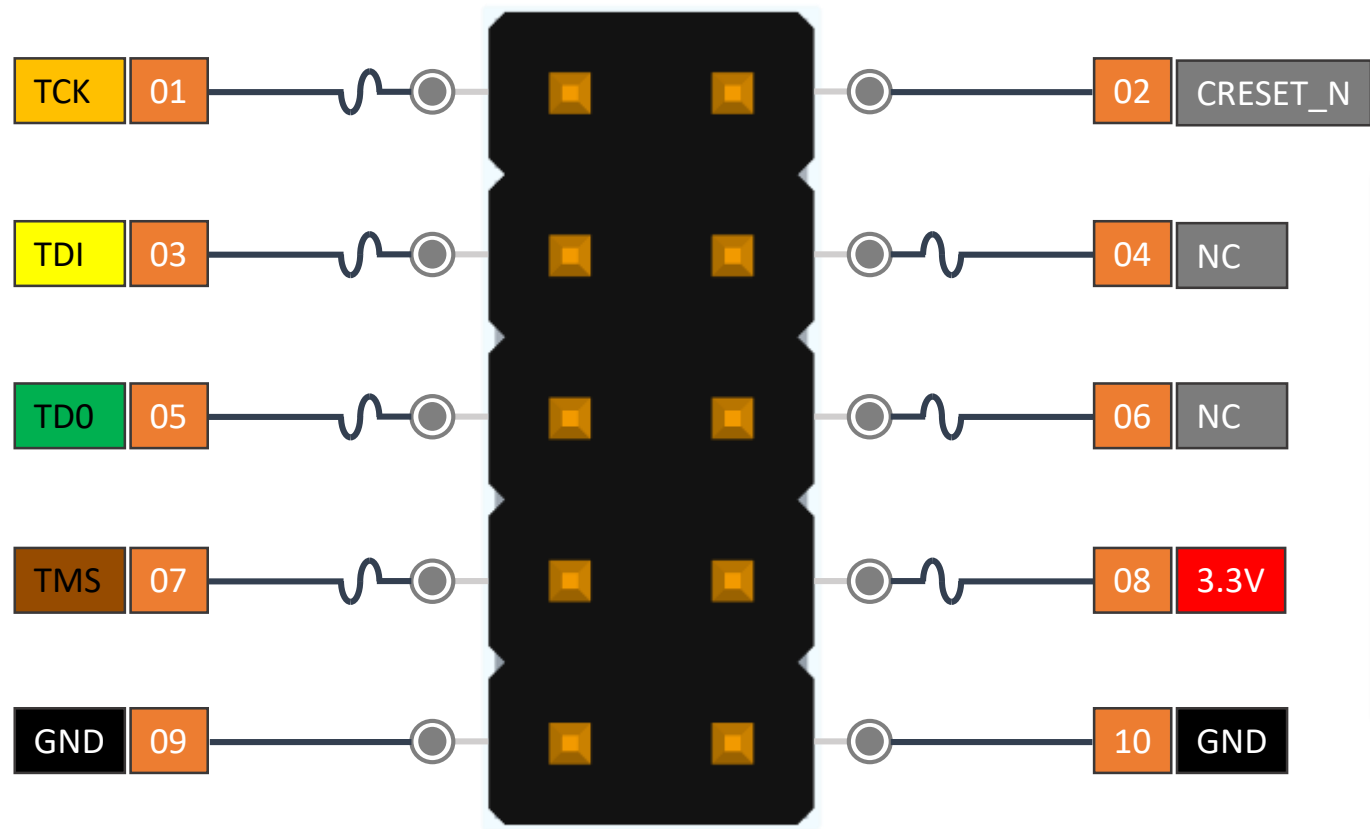


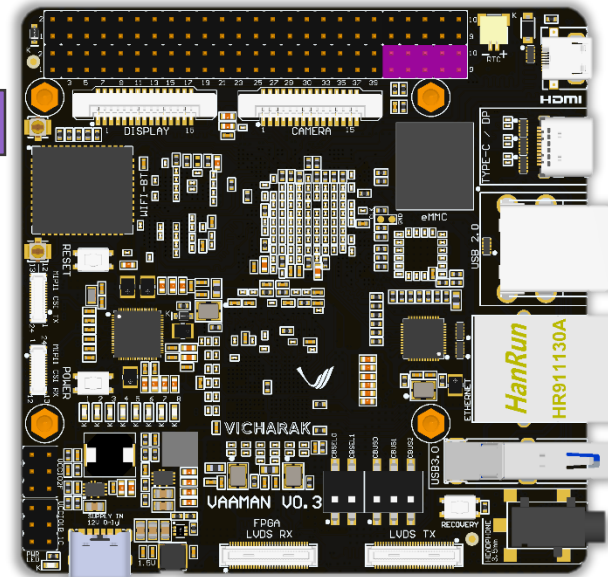
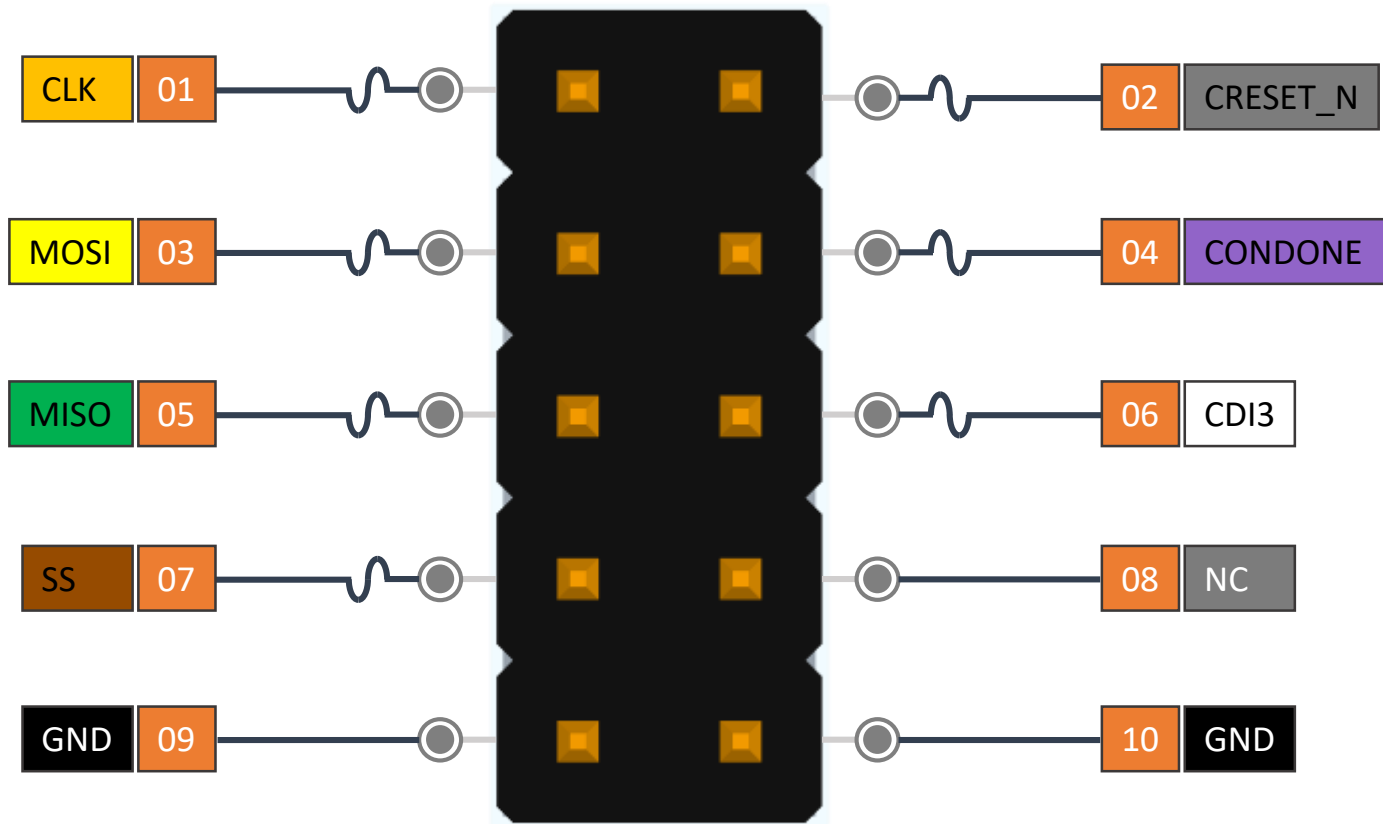
TYPE-C(USB3.0) / DisplayPort



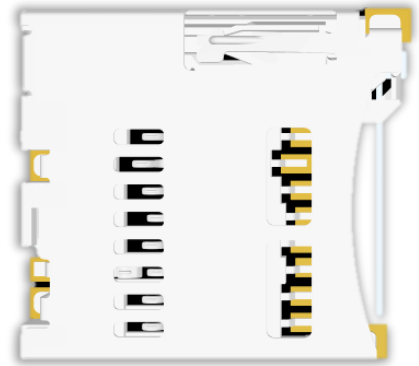




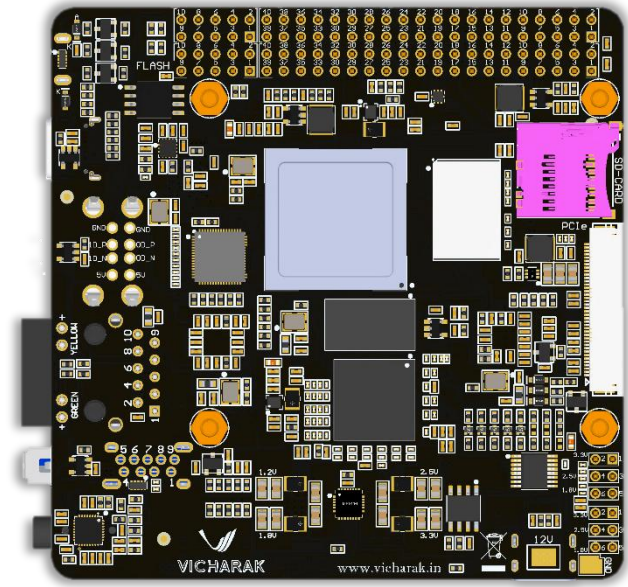


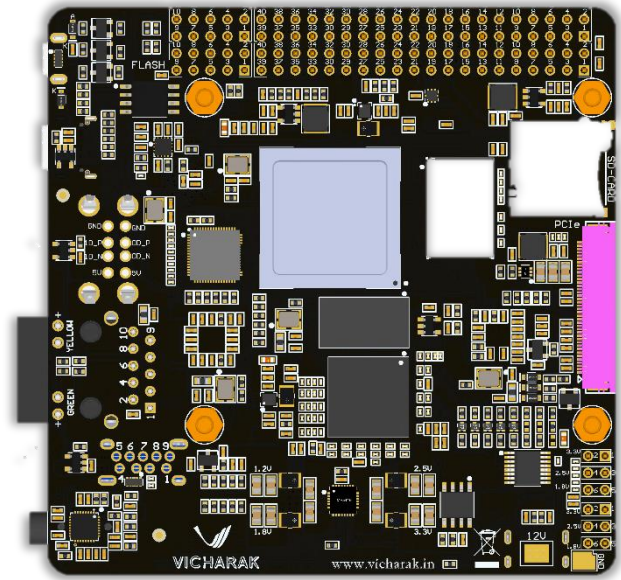
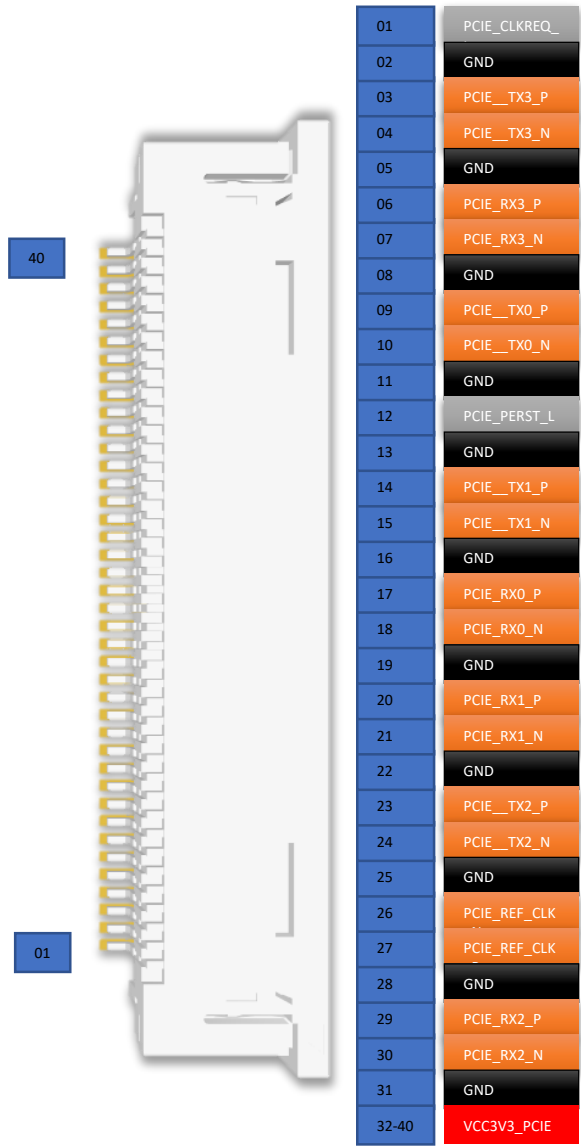


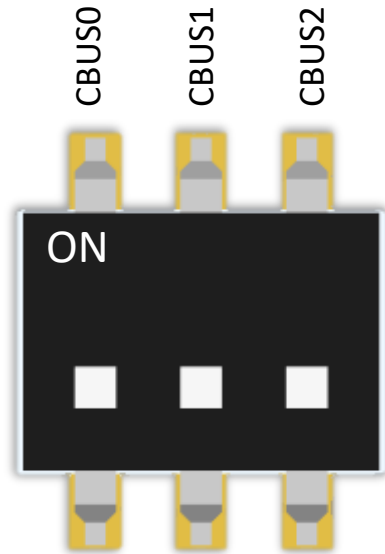




MicroSD Card







**Table 5: SPI Hardware Settings**

If you do not make any connections, the default mode is x1 SPI active.

Configuration Mode	Parallel/Serial	TEST_N	SS_N	CBUS2, CBUS1, CBUS0	Width
SPI Active	Serial	1	1	3'b111	x1
	Parallel	1	1	3'b110	x2
	Parallel	1	1	3'b101	x4
SPI Passive	Serial	1	0	3'b111	x1
	Parallel	1	0	3'b110	x2
	Parallel	1	0	3'b101	x4
	Parallel	1	0	3'b100	x8
	Parallel	1	0	3'b011	x16
	Parallel	1	0	3'b010	x32

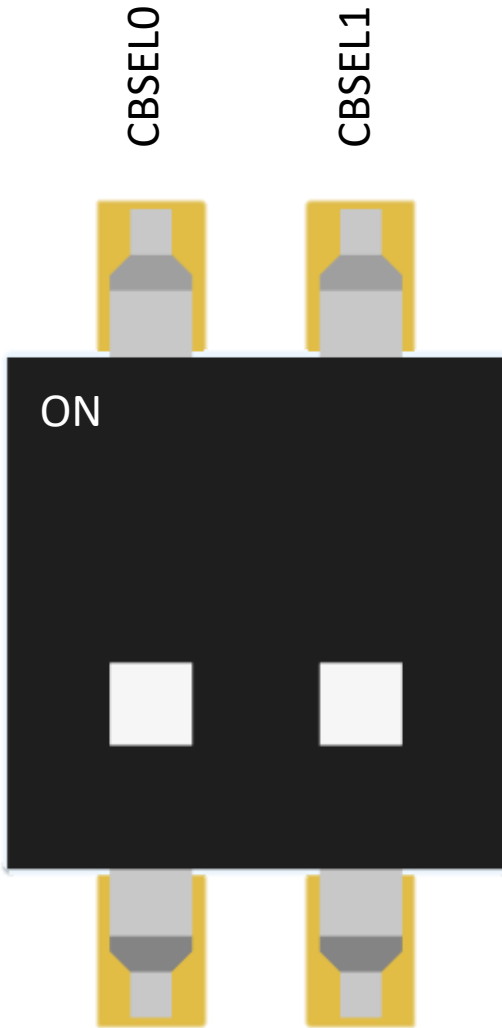
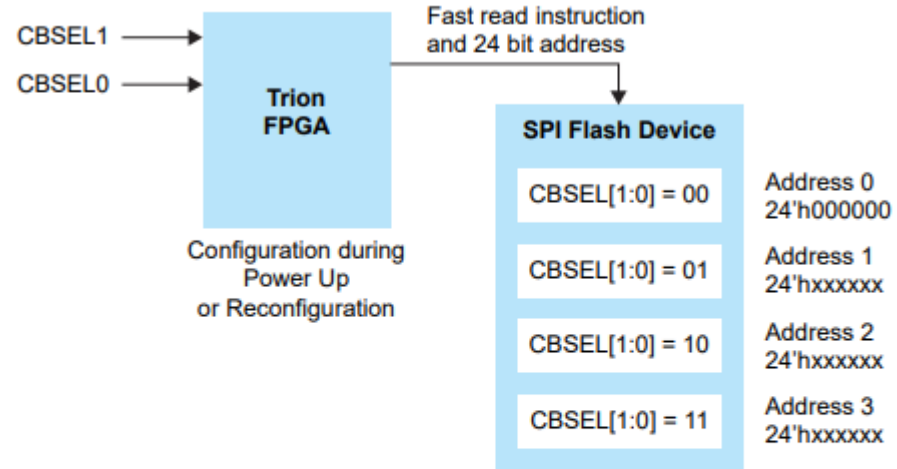


Figure 20: Configuration Setup for Multiple Images



Connect  $CBSEL[1:0]$  for the image you want to use:

- 00 for image 1
- 01 for image 2
- 10 for image 3
- 11 for image 4

You use the Efinity Programmer to combine multiple images into a single hex file.

**Note:** If the flash device does not have a valid image in the location the FPGA expects based on the  $CBSEL[1:0]$  setting, the FPGA looks at the image locations in ascending order until it finds a valid image. For example, if  $CBSEL[1:0]$  is 11 and the flash device has images for 00 and 01, the FPGA loads the image at 00.

# FPGA Internal Clock Sources

